Improving existing methods for stable and more accurate Power Hardware-in-the-Loop experiments

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***Abstract*—This paper deals with stability and accuracy issues that occur in Power Hardware-in-the-Loop experiments (PHIL). Firstly, based on the Bode stability criterion, an analytical investigation of the stability margins of a PHIL simulation without using approximations for the time delay is presented. Then, the proposed analysis is used for the extension of existing methods, which results in the accurate and justified choice of their parameters and, thus, the improvement of the accuracy and stability in PHIL experiments. Finally, the calculated parameters of the feedback filter method are compared with the real parameters derived from the execution of PHIL experiments.**

***Keywords*—power hardware in the loop, real-time simulation, time delay, bode stability criterion, feedback filter, shifting impedance method.**

I. INTRODUCTION

Power Hardware-in-the-Loop (PHIL) is a method that is used for testing a hardware power component in realistic conditions, while a part of the system is simulated in a Digital Real Time Simulator (DRTS). PHIL techniques are being increasingly used in the research community and industry. Some of the main advantages of PHIL testing are the safe and repeatedly testing of a Hardware-Under-Test (HUT) in faulty and extreme conditions without stressing/damaging laboratory equipment, the thorough study of transient and steady state operation of the HUT, the flexibility in choosing part of the test parameters and components among other. Therefore, the PHIL approach has been successfully applied in a variety of domains such as motor drives [1]-[3], distributed generation [4] -[12], electric ships [13] etc.

The DRTS is connected with the HUT via a power interface, which is usually a linear or a switched-mode amplifier, accompanied with a sensor. Generally, the amplifier inserts into the system time delays, noise and also affects the magnitude and phase of the signal under amplification due to its limited bandwidth. However, the inserted time delay is the main problem in a PHIL test as it can destabilize the system and decrease the accuracy of the experiments.

Several methods have been proposed in literature in order to deal with the time delay. For example, adding a low pass filter in the feedback loop [12], [14] is one of the most common techniques due to its simplicity. Another method proposes the use of high pass filters parallel to the input and the output of the power amplifier [15]. In [16] the shifting of a part of the simulated system in the hardware side is proposed, while in [12] an inductance is simply added in the hardware. Other techniques aim to compensate the time delay using digital first order approximation of lead functions [17] or to decompose the original signal and recompose it with different phase equal to the desired one [18]. The use of different sample times in simulation is also proposed [19]. Different Interface Algorithms (IA) are also presented in [22]. One of the most promising, is the Damping Impedance Method. Improvements of this method in order to increase the accuracy of a PHIL simulation and enhance its stability are proposed in [23]-[26]. Finally, Lauss et al. present a brief and comprehensive review of power hardware-in-the-loop (PHIL) simulations that are used for designing, analyzing, and testing of electrical power system components [27].

Although some of the proposed methods seem to achieve stable and satisfactorily accurate results, the choice of the parameters is not clear even for the simplest methods. Furthermore, some methods use approximation of the time delay, which in some cases, can lead to unstable conditions [20] or lower accuracy. In addition, trial and error techniques for choosing the parameters and commonly the lack of a guideline for using some of the aforementioned methods can make their application in other cases difficult.

The contribution of this paper is that it clarifies the stability boundaries of the parameters of a PHIL test with an analytical and accurate way without the common practice of approximating the time delay. Moreover, the implementation of the proposed analysis in existing methods, such as the introduction of a feedback filter and the shifting impedance method provide us with tools for the proper choice of the parameters in a well-structured way. Finally, the use of time delay as it is, namely, without any approximation, assures the stability and increases the accuracy of each method.

The structure of this paper is as follows: Section II analyzes the stability of a general PHIL interface method using the Bode stability criterion [21] and provides us with several quantitative results and parameter correlations of simple examples. In Section III the implementation of the proposed analysis in existing stability methods presented in [12] and [14], [16] in order to accurately and properly choose their parameters is described. In Section IV, the results of the PHIL experiments that validates the proposed mathematical analysis are also presented. Section V concludes this paper.

II. STABILITY ANALYSIS

A. PHIL Simulation Model

Generally, a PHIL system consists of a simulated part, a real one and the amplifier, which, as previously mentioned, affects the entire system with many ways. Before the execution of a PHIL experiment the stability and the accuracy of the system should be examined theoretically and in a simulated environment.

All parts of a PHIL system are usually represented in the frequency domain using the Laplace transformation of the time domain. The Laplace transformation can be used if linear systems or linear approximations of nonlinear systems are studied. A general transfer function representation of a PHIL system is shown in Fig 1.

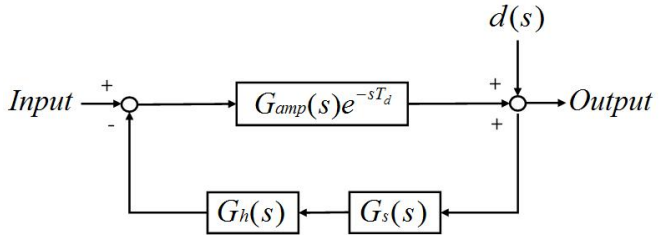

Fig 1. General representation of a PHIL system

where $G_s(s)$, $G_{amp}(s)$ and $G_h(s)$ are the transfer functions of simulated part, amplifier and hardware part respectively and the exponential term is the representation in the frequency domain of the time delay inserted by the amplifier. The disturbance inserted into the system due to extrinsic factors is symbolized as d(s). Taking into account un-modeled dynamics and uncertainties of the hardware components in the previous representation, the transfer function of the hardware component can be written as:

$$G_h(s) = G_{h\_nom}(s)(1 \pm \Delta(s)) \tag{1}$$

where $G_{h\_nom}(s)$ is the nominal transfer function of the hardware component and $\Delta(s)$ represent the un-modeled dynamics that satisfy the following inequality:

$$|\Delta(s)| \le \varepsilon \text{ and } \varepsilon > 0 \tag{2}$$

The assumption above will be used in the following subsection where the stability conditions will be analyzed.

B. Stability Conditions(Bode criterion)

In order to increase the accuracy of the results, while maintaining the stability of the entire system, it is important to use simple methods for the stability examination. In addition, avoiding approximating techniques for the representation of the time delay is important for an accurate analysis of the stability issue. Bode stability criterion [21] enables us to study the open loop system and extract important conclusions for the closed loop system.

According to the Bode stability criterion and based on the presented PHIL model the following conditions should be satisfied:

$$\left|G_s(s)G_{amp}(s)e^{-sT_d}G_h(s)\right| \le 1 \tag{3a}$$

And

$$\angle G_s(s) + \angle G_{amp}(s) + \angle G_h(s) - \omega T_d = \pi \tag{3b}$$

Furthermore, taking into consideration uncertainties and un-modeled dynamics of the hardware component and using equations (1), (2) the stability conditions can be rewritten in a more conservative way as follows:

$$\begin{aligned} &\left|G_s(s)G_{amp}(s)e^{-sT_d}G_{h\_nom}(s)(1+\Delta(s))\right| \le 1 \Rightarrow \\ &\Rightarrow \left|G_s(s)G_{amp}(s)e^{-sT_d}G_{h\_nom}(s)\right|\left|(1+\Delta(s))\right| \le 1 \Rightarrow \\ &\Rightarrow \left|G_s(s)G_{amp}(s)e^{-sT_d}G_{h\_nom}(s)\right|(1+\varepsilon) \le 1 \Rightarrow \\ &\Rightarrow \left|G_s(s)G_{amp}(s)e^{-sT_d}G_{h\_nom}(s)\right| \le 1/(1+\varepsilon) \end{aligned} \tag{3c}$$

Equation (3c) implies that we should choose a more conservative condition for the magnitude of the open loop system under an uncertain environment. Although, this is an expected result, (3c) quantifies the limits within the system can lie and correlates these limits with the maximum magnitude of the uncertainties and un-modeled dynamics (if the latter are known and bounded).

C. Applications of the proposed method

In this subsection simple applications of the proposed method are presented. A simple PHIL simulation system of a voltage divider is assumed. The simulated part is a voltage source and a line with R_s and L_s elements, while the hardware part an RL load. It is also assumed that the amplifier has unity gain but inserts into the system a time delay (T_d). Here, the effect of the time delay as well as the relation between the simulated and hardware parts on the system's stability is analyzed. Different cases for the systems components are examined. The applied PHIL system is presented below:

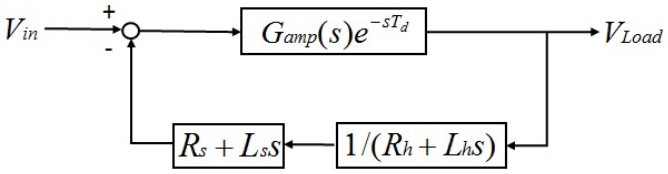

Fig 2. Real system representation

The closed loop transfer function of the system in Fig 2 is as follows:

$$T_{CL} = \frac{G_{amp}(s)e^{-sT_d}(R_h + L_h s)}{(R_h + L_h s) + G_{amp}(s)e^{-sT_d}(R_s + L_s s)} \tag{4a}$$

In (4a) the effect of the time delay is clearer and as it is positioned in the denominator it becomes in many cases the cause of the instability in the system. Assuming that $G_{amp}(s) = 1$ for all frequencies (4a) gives:

$$T_{CL} = \frac{e^{-sT_d}(R_h + L_h s)}{(R_h + L_h s) + e^{-sT_d}(R_s + L_s s)} \tag{4b}$$

In the previous subsection, it is shown that for the examination of the system's stability the open loop stability conditions are only required. Consequently, taking into account that the open loop system of Fig 2 is given by:

$$T_{OL} = \frac{(R_s + L_s s)}{(R_h + L_h s)} e^{-sT_d} \tag{5}$$

the presented PHIL system stability conditions become as follows:

$$\left| \frac{(R_s + L_s s)}{(R_h + L_h s)} e^{-sT_d} \right| \le 1 \tag{6a}$$

$$\angle(R_s + L_s s) - \angle(R_h + L_h s) - \omega T_d = \pi \tag{6b}$$

Equations (6a) and (6b) can also be written as:

$$\sqrt{\frac{R_s^{\,2} + L_s^{\,2}\omega^2}{R_h^{\,2} + L_h^{\,2}\omega^2}} \le 1 \tag{6c}$$

$$\arctan\left(\frac{\omega L_s}{R_s}\right) - \arctan\left(\frac{\omega L_h}{R_h}\right) - \omega T_d = \pi \tag{6d}$$

Based on (6c) and (6d) the stability conditions for different values of the system's parameters are examined. Here, four different cases are presented. In all cases the existence of a variety of time delays (T_d) is assumed. From a practical point of view, the charts below figure the values of the simulated components and the time delay that should be chosen using certain hardware components in order to achieve stability.

1) R_s line, R_h load

In this case, the open loop transfer function becomes:

$$T_{OL\_1} = \frac{R_s}{R_h} e^{-sT_d} \tag{7a}$$

And the stability condition as follows:

$$\frac{R_s}{R_h} \le 1 \tag{7b}$$

From the above inequality, it is obvious that in the case of only pure resistances, a PHIL system is stable if the resistance of the hardware R_h is larger than the resistance of the software R_s (as already shown in [22]). Furthermore, it is shown from (7b) that the system is independent of the time delay.

2) R_s line, R_h - L_h load

In this case it is assumed that the line consists only of R_s resistance, while the load consists of a resistance R_h and an inductance L_h connected in series. The open loop transfer function becomes:

$$T_{OL\_2} = \frac{R_s}{R_h + sL_h} e^{-sT_d} \tag{8a}$$

While the stability conditions are:

$$\frac{R_s}{\sqrt{R_h^{\,2} + L_h^{\,2}\omega^2}} \le 1 \tag{8b}$$

$$-\arctan\left(\frac{\omega L_h}{R_h}\right) - \omega T_d = \pi \tag{8c}$$

Solving the pair of equations (8b) and (8c) above we calculate the maximum simulated resistance R_{s_max} that can be tolerated by the system without causing stability issues. The chart below shows the variation of resistance R_s with respect to the hardware resistance R_h and the hardware inductance L_h for different time delays T_d. In the first case, it is assumed that L_h = 1 H, while in the second, R_h = 1 Ohm.

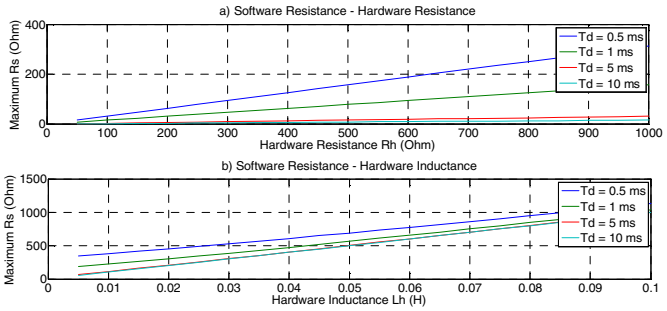

Fig 3. Variation of the software resistance with respect to a) hardware resistance and b) hardware inductance for different time delays

From the chart above we observe that an increase in both hardware resistance R_h and inductance L_h cause an increase in the maximum tolerated software resistance. However, the hardware inductance L_h affects more significantly the maximum tolerated software resistance. Finally, an increase in time delay T_d, limits the bounds from which the maximum tolerated software resistance could be chosen.

3) R_s - L_s line, R_h - L_h load

In this case it is assumed that both the line and the load consist of a resistance and an inductance respectively. So, the open loop function of the system becomes as in (5) and the stability conditions as in (6c) and (6d). The first chart below shows the software resistance R_s variation with respect to the hardware inductance R_h and the time delay T_d while L_s = 0.005 H and L_h = 1 H. The second chart shows the software resistance R_s variation with respect to the hardware inductance L_h and the time delay T_d while R_h = 1 Ohm and L_s = 0.005 H.

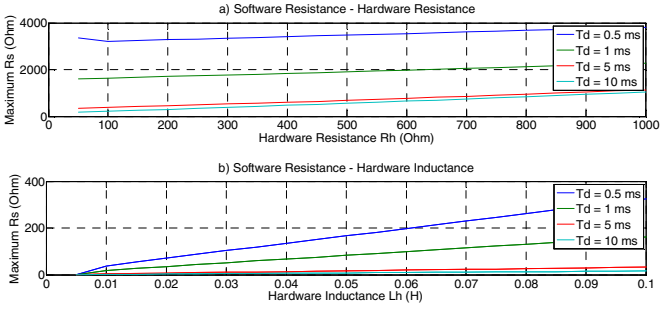

Fig 4. Software resistance variation with respect to a) hardware resistance and b) hardware inductance for different time delays

The results are similar with the previous subsection. However, due to the existence of the software inductance L_s, both hardware resistance R_h and inductance L_h, weakly affect the software resistance R_s.

4) Maximum Time delay Calculation

In this case, it is assumed that the hardware components of the PHIL simulation are constant. The maximum time delay that can be tolerated by the system in order to remain stable is calculated using the stability condition (6c) and (6d). The open loop transfer function is given by (5). The charts below show the maximum time delay (T_d) variation with respect to the software resistance R_s and the software inductance L_s.

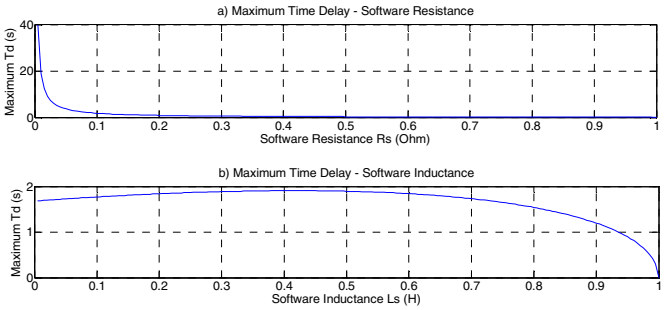

Fig 5. Maximum time delay variation with respect to a) Software resistance Rs b) Software inductance Ls

At the first chart it is assumed that L_s = 0.05 H, L_h = 0.1 H and R_h = 0.001 Ohm, while at the second one R_s = 1 Ohm H, L_h = 1H and R_h = 0.1 Ohm. As expected, an increase in the software resistance decreases drastically the margins of the maximum time delay. However, the second chart shows a more complex relation between the time delay and the software inductance when the time delay reaches a peak at 0.4 H and decreases rapidly until 1H.

III. Proposed Analysis Applied to Existing Methods

In this section, two existing methods for PHIL stability are analyzed. The first method adds a low pass filter in the feedback loop of the measured current (Feedback Filter) while the second one (Shifting Impedance Method) shifts a part of the simulated component in the hardware side. Furthermore, the authors of the Shifting Impedance Method provide a mathematical proof for the choice of the software inductance in case of the voltage divider. However, in a general case, none in the literature presents a clear guideline for choosing the stability methods' parameters in order to run an experiment in the safe side. So, a quantification for choosing the methods' parameters is attempted here. The initial PHIL test have already presented in Fig 2 and is assumed unstable. For this, the use each of the aforementioned stability methods is required.

A. *Feedback filter [12],[14]*

In this case, the model of Fig 2 has changed and is shown below:

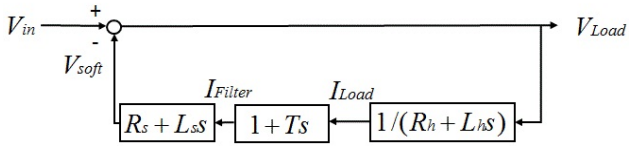

Fig 6. PHIL model with feedback filter

The open loop transfer function of the new model is given by:

$$T_{OL\_filter} = \frac{(R_s + L_s s)}{(R_h + L_h s)(1 + sT)} e^{-sT_d} \quad (9a)$$

While the stability conditions as follows:

$$\sqrt{\frac{R_s^2 + L_s^2\omega^2}{(R_h^2 + L_h^2\omega^2)(1 + \omega^2 T^2)}} \le 1 \quad (9b)$$

$$\arctan\left(\frac{\omega L_s}{R_s}\right) - \arctan\left(\frac{\omega L_h}{R_h}\right) - \arctan(\omega T) - \omega T_d = \pi \quad (9c)$$

Solving the above pair of equations the maximum cut-off frequency of low pass filter that stabilizes the system is received. The chart below shows the variation of the maximum frequency of the low pass with respect to R_s and L_s.

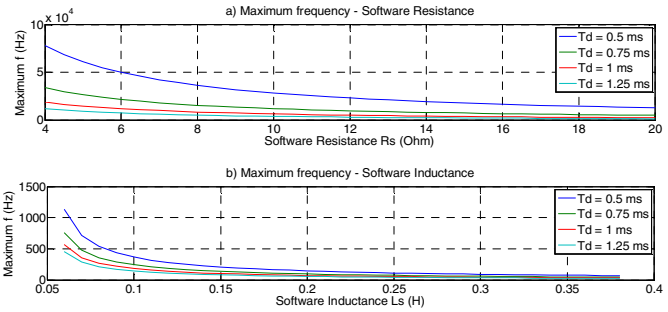

Fig 7. Maximum frequency variation of the low pass filter with respect to the a) software resistance and b) software inductance for different time delays

The constant parameters for the first chart are L_s = L_h = 0.05 H and R_h = 1 Ohm while for the second one are R_s = R_h = 1 Ohm and L_h = 0.05 H. It is shown that the region over the line leads the system to instability. In addition, it is obvious that the software inductance affects the choice of the low pass filter more drastically than the software resistance. The increase of both, leads to a more restrict choice of the low pass filter that means less accuracy for the PHIL experiment.

B. *Shifting Impedance Method (SIM) [16]*

In this method, the authors propose the shifting of a part of the simulated system in the hardware side and apply their method in a voltage divider. The authors of [16] estimate correctly the minimum shifted inductance L_{sh}, however, the

minimum software resistance R_{sh} is approximated. Here, the model of Fig 2 has changed and is shown below:

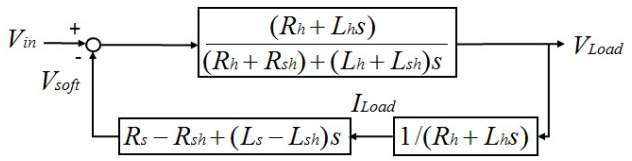

Fig 8. PHIL model with shifting impedance method

The open loop transfer function of the new model is given by:

$$T_{OL\_shifting} = \frac{R_s - R_{sh} + (L_s - L_{sh})s}{R_h + R_{sh} + (L_h + L_{sh})s} e^{-sT_d} \quad (10a)$$

Where R_{sh} and L_{sh} are the part of the software component that should be shifted into the hardware in order the system to be stable.

The stability conditions are as follows:

$$\sqrt{\frac{(R_s - R_{sh})^2 + (L_s - L_{sh})^2 \omega^2}{(R_h + R_{sh})^2 + (L_h + L_{sh})^2 \omega^2}} \le 1 \quad (10b)$$

$$\arctan\left(\frac{\omega(L_s - L_{sh})}{R_s - R_{sh}}\right) - \arctan\left(\frac{\omega(L_h + L_{sh})}{R_h + R_{sh}}\right) - \omega T_d = \pi \quad (10c)$$

Solving the above pair of equations, the minimum amount of software component that should be shifted is received. The chart below shows the variation of the shifted resistance R_{sh} with respect to the shifted inductance L_{sh}. The constant parameters are L_s = 5 kOhm, R_h = 200 Ohm, L_s = 0.1 H and L_h = 0.05 H.

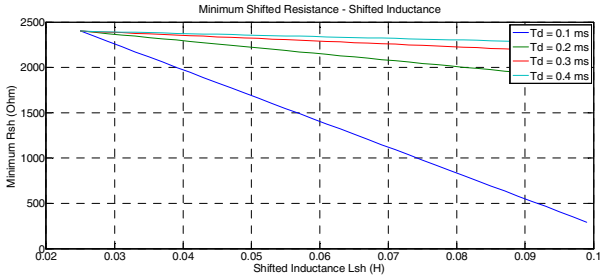

Fig 9. Minimum shifted resistance variation with respect to a certain amount of shifted inductance.

From the chart above it is concluded that a small amount of shifted inductance L_{sh} has a great effect in the choice of the shifted resistance R_{sh}. Note that for a significant change in the shifted inductance L_{sh} no need for change in the software resistance R_s is required. On the other hand, an amount of hardware resistance could be potentially shifted from the hardware component to the software one.

Applying the proposed method on the PHIL system of [10] it is proved that no software resistance is needed to be transferred. This leads to much higher accuracy in the whole frequency bandwidth, as shown in the next chart.

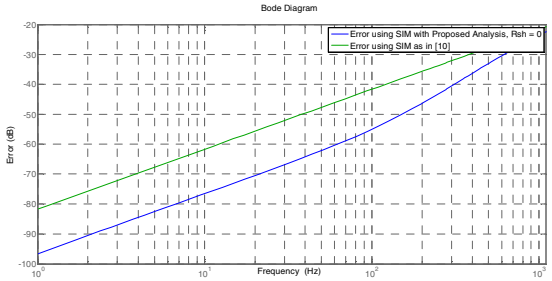

Fig 10. Accuracy of a PHIL simulation using Shifting Impedance Method (with and without applying the proposed analysis)

IV. PHIL Experiments

In this section, PHIL experiments are realized. Based on the previous approach, the transfer function of the power amplifier is also taken under consideration. Now, the initial system is assumed unstable. In order to achieve stability the feedback filter method is applied.

The implemented setup includes a DRTS, a linear amplifier and a resistive load. Furthermore, a current sensor and the appropriate digital to analog and analog to digital converters for the reception and the sending of the DRTS signals are also used. The setup is shown below in Fig 10.

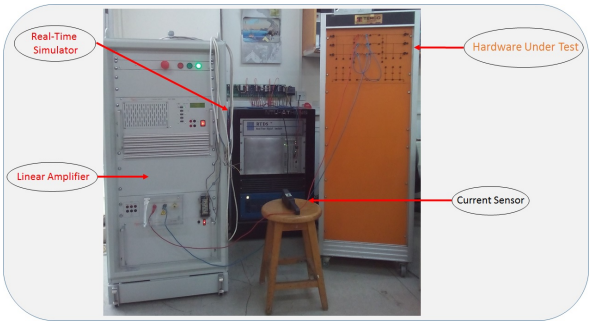

Fig 11. PHIL Setup

In all the experiments the circuit of the voltage divider is examined and two different main cases are assumed. In the first case, a resistor R_s is simulated and a resistive load R_h is used as HUT, while in the second one an R-L line is simulated using the same resistive load R_h again. In all cases, the systems that are tested are, at first, unstable. As a result, a method to achieve stability is needed. We choose to use the simplest one, which is the feedback filter, and based on the previous analysis we calculate the value of the cut-off frequency of the appropriate filter. Then, this filter is applied on the PHIL setup and its stability is examined. The real cut-off frequency of the filter is found when instability marginally occurs. Practically, the activation of the software protections in the DRTS shows the marginal stability. The figure below shows the calculated and the real values of the used feedback filter.

In this case two different loads are used, 15.9 and 10.6 Ohms respectively, while changes in software resistance are applied.

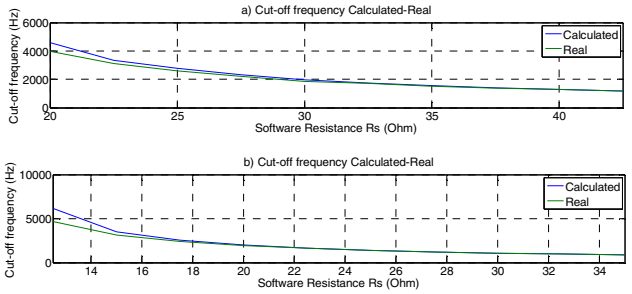

Fig 12. Calculated and real cut-off frequency of the low pass filter-Case 1

In the second case, two different values for the software inductance Ls are used, 1 mH and 0.1 mH respectively, while the resistive load remains constant at 15.9 Ohms. Again, changes in software resistance Rs are applied. Fig 13 shows the changes in the calculated and real cut-off frequency of the feedback filter.

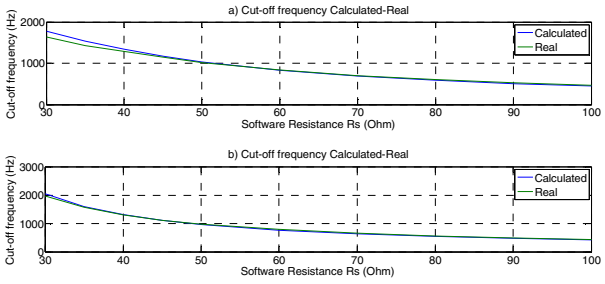

Fig 13. Calculated and real cut-off frequency of the low pass filter-Case 2

In both cases it is observed that the results of the PHIL experiments are quite satisfactory as the errors between the real and the calculated values of the cut-off frequency of the feedback filter are below 5%, especially when the cut-off frequency is lower than 2 kHz. In some cases where the calculated frequency is lower than 1 kHz the error is drastically reduced, less than 0.5%. However, as the values of the cut-off frequency increase the error also increases rapidly. This can be explained satisfactorily due to the fact that the model we calculated for the linear amplifier is not so accurate in high frequency phenomena. Furthermore, the linear amplifier used is able to reproduce periodical signals with maximum frequency of 5 kHz, which affects negatively the system's operation when instability phenomena near to this frequency are examined, as in this case. Last but not least, the impact of the current sensor (phase lag of the measured signal) and the communication/meter cables (no shielded cables pick up noise) is not taken into account due to the difficulty to be modelled. As a result, noise and changes in the phase of the signal become more obvious in high frequencies.

V. CONCLUSION

In this paper, an analytical and accurate method to determine the marginal parameters of a PHIL experiment using the Bode stability criterion is proposed. The proposed analysis is applied to existing methods (i.e. feedback current filter, shifting impedance method) to achieve stability and the accurate selection of parameters is made possible. Specifically, the marginal cut-off frequency of the feedback filter method is calculated. Moreover, it is proved that, in the shifting impedance method, the shifted resistance required to achieve stability is less than that it is proposed in [16] and its value is calculated. It is also proved that the proposed method leads to much higher accuracy in the PHIL experiments. The parameters' calculation for the feedback filter method is also validated running PHIL experiments in NTUA's laboratory. Comparative charts for calculated and real cut-off frequency are also presented. Future work will focus on applying the proposed analysis in other stability methods and Interface Algorithms, such as the Damping Impedance Method, using more complex hardware under test and running a larger number of PHIL experiments.

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